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HTC CORPORATION and
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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOTIC SCIENTIFIC CORPORATION and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-CV-00882 JF

(Related to Case Nos. C-08-05398 JF and C-08-00877 JF)

HTC'S NOTICE OF MOTION AND MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF U.S. PATENT NOS. 5,440,749, 5,809,336 AND 6,598,148; MEMORANDUM OF POINTS AND AUTHORITIES

Date: [TBD]
Time: [TBD]
Place: Courtroom 3, 5th Floor
Judge: Hon. Jeremy Fogel

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NOTICE OF MOTION AND MOTION

PLEASE TAKE NOTICE that Plaintiffs HTC Corporation and HTC America, Inc. (collectively "HTC") move, pursuant to Federal Rule of Civil Procedure 56, for summary judgment (1) that the accused HTC Faraday 2125, Iris S640, PC Advantage X7501, Apache XV6700, S621, Shadow, Star Trek 3125, Tilt TYTN II, Touch Dual, XV6600, Wing, Mogul XV6800, P4351, PDA i-mate, P3600, Dash, P3300, P3470, P4300, PDA2K, S710, TYTN, Wizard, S720, SPV C500/SMT 5600, Tornado, Touch Cruise P3650, Touch Phone Diamond and Touch Phone Touch (collectively the "accused '749 products") do not infringe any asserted claim of U.S. Patent No. 5,440,749 (the "'749 patent"); (2) that the accused HTC Dash, P4000, P4300, P4351, S621, S630, S640, S710, S720, S730, Shadow, Star Trek 3125, Tornado, Touch Phone Diamond, Touch Phone Fuze, Touch Phone P3650, Typhoon, Wing, Wizard, and Titan XV6800 (collectively the "accused '336 products") do not infringe any asserted claim of U.S. Patent No. 5,809,336 (the "'336 patent"); (3) that the accused HTC X7501, P3470 and P3300 (collectively the "accused '148 products") do not infringe any asserted claim of U.S. Patent No. 6,598,148 (the "'148 patent") ("Motion").

This Motion is filed pursuant to the briefing schedule established by the Court's order of March 23, 2011 as amended on April 7, 2011. Doc. Nos. 279, 290. The Court did not set a hearing date for HTC's Motion so no hearing date is provided in this Notice. This Motion is based on the Memorandum of Points and Authorities set forth below, the supporting declaration of Kyle D. Chen ("Chen Decl.") and exhibits thereto, and such other matters as may be presented at the hearing on HTC's motion and allowed by the Court.

MEMORANDUM OF POINTS AND AUTHORITIES

I. INTRODUCTION

TPL has improperly accused features and elements of HTC's accused products that TPL specifically disclaimed during the reexaminations of the '749, '336 and '148 patents in order to obtain allowance of its claims. Because TPL's claims cannot be construed to recapture subject matter it disclaimed, HTC cannot infringe, and summary judgment of non-infringement should be granted with respect to the accused '749, '336 and '148 products listed above.

II. LEGAL STANDARD

Evaluating claims of patent infringement involves a two-step process. First, the Court construes the claims as a matter of law. *See Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000). "Second, the claims, as construed, are compared to the accused device." *Id.* The absence of even a single claim limitation from the accused device precludes a finding of infringement. *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1330 (Fed. Cir. 2001). As the party asserting patent infringement, TPL bears the burden of establishing that the accused products satisfy each element of each asserted claim. *Id.*

The summary judgment procedure is designed to dispose of specious claims and to avoid unnecessary trials. *See Celotex Corp. v. Catrett*, 477 U.S. 317, 327 (1986). Federal Rule of Civil Procedure 56 requires entry of summary judgment where there is no genuine issue as to any material fact and the moving party is entitled to judgment as a matter of law. *See* Fed. R. Civ. P. 56(a), (c)(2). "Summary judgment is as appropriate in a patent case as it is in any other case." *Desper Prods., Inc. v. QSound Labs, Inc.*, 157 F.3d 1325, 1332 (Fed. Cir. 1998). "Summary judgment of non-infringement is appropriate where the patent owner's proof is deficient in meeting an essential part of the legal standard for infringement, since such failure will render all other facts immaterial." *Telemac Cellular Corp.*, 247 F.3d at 1323.

Federal Circuit law is clear that when there are no factual disputes regarding the operation of the accused products, the question of literal infringement collapses into a legal question of claim construction that can be resolved as a matter of law on summary judgment. *See, e.g., MyMail, Ltd. v. Am. Online, Inc.*, 476 F.3d 1372, 1378 (Fed. Cir. 2007) ("Because there is no dispute regarding the operation of the accused systems, that issue [of literal infringement] reduces to a question of claim interpretation and is amenable to summary judgment."); *see also General Mills, Inc. v. Hunt-Wesson, Inc.*, 103 F.3d 978, 983 (Fed. Cir. 1997).

The operation of the accused products, for purposes of this motion, is based on TPL's own description of those products as set forth in its Infringement Contentions (to which TPL is bound). This Court has made clear that summary judgment of non-infringement may be based entirely on the patentee's own description of the accused products as set forth in its Infringement

Contentions. *See Berger v. Rossignol Ski Co., Inc.*, No. C 05-02523 CRB, 2006 WL 1095914, at *5-6 (N.D. Cal. April 25, 2006) (granting summary judgment of non-infringement based on admissions about the accused product contained in plaintiff's infringement contentions).[1]

III. ARGUMENT

A. The Accused '749 Products Do Not Infringe the '749 Patent.

1. Background of the '749 Patent

The '749 patent purports to describe a high-performance low cost microprocessor system. '749, 1:7-13. The central processing unit ("CPU") described in the '749 patent operates by fetching "instructions" from memory and then executing them. These fetched instructions specify the operations the CPU will perform. The '749 patent explains, however, that "[t]he slowest procedure the microprocessor 50 performs is to access memory." '749, 22:14-17. "Memory is accessed when data is read or written. Memory is also read when instructions are fetched." *Id.* "The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data." '749, 5:54-56.

The '749 patent purports to address this "bottleneck" problem through a microprocessor system that has the ability to fetch *multiple* instructions from memory and supply them to the CPU during "a single memory cycle," *i.e.*, the period of time required to perform one memory access. Because the CPU can execute instructions much faster than it can fetch them from the memory, allowing multiple instructions to be fetched and supplied to the CPU during a single memory cycle can improve performance by permitting the fetching and execution of instructions to take place in parallel. *See* '749, 22:17-40. The specification of the '749 patent repeatedly touts the perceived advantages of this feature. '749, 18:10-12 ("The microprocessor 50 fetches up to

[1] The non-infringement arguments articulated in this Motion were selected because they relate to the pending claim construction disputes and are based entirely on TPL's own admissions reflected in its Infringement Contentions and the prosecution history of the reexaminations of the '749, '336 and '148 patents. HTC has identified other grounds for non-infringement beyond those articulated in this Motion, but as those grounds may require evidence or documents more than TPL's Infringement Contentions, HTC reserves its right to bring additional dispositive motions after claim construction to the extent any aspects of TPL's infringement claims under the '749, '336 and '148 patents remain following the disposition of this Motion.

four instructions in a single memory cycle and can perform much useful work before requiring another memory access."); *see also, e.g.*, 7:12-18; and 5:54-58.

Each of the two asserted independent claims of the '749 patent (*i.e.*, claims 1 and 9) includes a substantially identical limitation directed at this feature. In particular, each independent claim requires that the microprocessor system be configured to fetch multiple sequential instructions in parallel and *supply them to the CPU during a single memory cycle*. Claim 1 of the '749 patent, for example, reads in its entirety:

> 1. A microprocessor system, comprising a central processing unit integrated circuit, a memory extend of said central processing unit integrated circuit, a bus connecting said central processing unit integrated circuit to said memory, and means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and **supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle**, said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel, said central processing unit including an arithmetic logic unit and a first push down stack connected to said arithmetic, logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack said arithmetic logic unit having an output connected to said means for storing a top item.[2]

'749, claim 1 (emphasis added). Claim 9, the other asserted independent claim,[3] contains

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[2] The claim 1 shown in the text is the currently-operative claim language as of the filing of this brief. TPL amended claim 1 in the reexamination of the '749 patent by adding new limitations (which will not be operative until the reexamination certificate issues), but those amendments are immaterial to this motion. The limitation, "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle," will remain an essential element of each independent claim after the reexamination certificate issues.

[3] Claim 9 has been cancelled during the reexamination, but its limitations, including the one at issue in this Motion, have been incorporated into the substituting and dependent claims to be

substantially the same requirement. *See* '749, claim 9 ("said means for fetching instructions being configured to . . . supply the multiple instructions to said central processing unit during a single memory cycle").

2. TPL Affirmatively Disclaimed Systems that Supply Instructions to the CPU One at a Time During the Reexamination.

On November 19, 2009, the PTO issued an Office Action in the reexamination rejecting various claims of the '749 patent (including claim 1) based on U.S. Patent No. 4,680,698 to Jonathan Edwards ("Edwards") and an article entitled *The Motorola MC68020* by Doug MacGregor et al. ("MacGregor"). As explained below, in attempts to distinguish Edwards and MacGregor, TPL unequivocally disclaimed systems that supply instructions to the CPU one-at-a-time by arguing that those systems do not "supply the multiple sequential instructions to the CPU during a single memory cycle," as required by the claims of the '749 patent. TPL is bound by those disavowals and, therefore, systems that operate in that manner cannot infringe the claims.

Specifically, on January 19, 2010, in its attempt to distinguish its claims over the prior art, TPL told the PTO that Edwards did not disclose this element because:

> Edwards describes the way the Transputer decodes and executes instructions. As described in Edwards, see, e.g., Fig. 8, below, instructions are supplied to a one-instruction-wide instruction buffer, one at a time, and are there decoded. Fetching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation – the supplying of "multiple sequential instructions to a CPU during a single memory cycle."

Amendment, 1/19/10, p. 26 of 58, Chen Decl., Ex. 1 (emphasis added). TPL made a similar disclaimer in distinguishing the claimed invention from MacGregor:

> However, [MacGregor] does not disclose fetching ['] multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle['']. MacGregor might imply that it fetches two instructions from memory at a time, but the instructions are supplied to the CPU one at a time. Such non-parallel supplying of instructions to the CPU is not supplying them to the CPU during a single memory cycle as required by the claim.

Id., p. 45 of 58.

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issued. Hence, all arguments still apply regardless of the cancellation.

On September 29, 2010, the PTO issued a final Office Action maintaining the rejection of claims 1 and 9. Shortly thereafter, TPL conducted an interview with the Examiner. Following that interview, TPL filed a written summary of its arguments and reaffirmed that systems supplying instructions to the CPU one at a time were *not* covered by the claims of the '749 patent:

> Next the MacGregor reference was discussed [during the interview]. Mr. Henneman [TPL's counsel] explained that although two instructions might be fetched at the same time, only one instruction is supplied to the CPU at a time. The second instruction is stored in a temporary register. Because MacGregor only discloses providing instructions to the CPU one-at-a-time, Examiner Pokrzwya indicated that he would reconsider this rejection.

Amendment, 11/29/2010, pp. 19-20 of 35, Chen Decl., Ex. 2 (emphasis added). Additionally:

> As discussed in the interview and elaborated on above with respect to the May/Edwards rejections, the "during a single memory cycle" limitation is not satisfied by supplying only one instruction to a CPU at a time. Rather, the "multiple sequential instructions" must be supplied "during a single memory cycle."

Id. at p. 31 of 35 (emphasis added). The PTO subsequently issued a Notice of Intent to Issue a Reexamination Certificate as to the '749 patent.

Each of TPL's disclaimers must be taken into account in a proper claim construction. "The purpose of consulting the prosecution history in construing a claim is 'to exclude any interpretation that was disclaimed during prosecution.'" *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) (citation omitted). "Accordingly, 'where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender.'" *Id.* (citation omitted); *see also, e.g., Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to narrow claim interpretations because 'the public has a right to rely on such definitive statements made during prosecution.'") (citation omitted).

The principle that a patent owner is bound to its representations to the PTO serves a critical purpose. "Such a use of the prosecution history ensures that claims are not construed one way in order to obtain their allowance and in a different way against accused infringers." *Chimie*, 402 F.3d at 1384. As such, the claim limitation "supply the multiple sequential instructions to

said central processing unit during a single memory cycle" must be construed as providing the multiple sequential instructions "in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle without using a prefetch buffer or a one-instruction-wide instruction buffer, that supplies one instruction at a time." Doc. No. 243, at 25:11-14.

3. TPL's Infringement Contentions Admit That the Accused '749 Products Supply Instructions to the CPU One at a Time.

As explained above, TPL plainly told the PTO that the requirement of supplying multiple sequential instructions to the CPU during a single memory cycle "is not satisfied by supplying only one instruction to a CPU at a time." Amendment, 11/29/2010, p. 31 of 35, Chen Decl., Ex. 2 (emphasis added). TPL's Infringement Contentions as to this element nonetheless affirmatively allege that the accused products supply instructions *one-at-a-time* to the CPU in precisely the same manner as the prior art TPL disclaimed in order to obtain allowance of its claims.

All of the products accused by TPL in this action use chips that incorporate microprocessor cores provided by a third party, ARM Ltd. ("ARM cores"). ARM cores, the alleged "central processing unit" according to TPL's infringement contentions, execute either 32-bit ARM instructions or a more compact instruction set referred to as "Thumb" instructions. Each Thumb instruction is 16-bits in length, such that two 16-bit Thumb instructions fit within a single 32-bit unit (known as a "word"). TPL claims that the accused products satisfy the element of supplying "multiple sequential instructions" to the CPU "during a single memory cycle" because they can fetch, during a single memory cycle, a 32-bit word containing two 16-bit Thumb instructions. But critically, TPL's infringement contentions go on to concede that these 16-bit instructions are supplied to the CPU one-at-a-time.

For example, in the cell of its infringement charts corresponding to the claim limitation, "supply the multiple sequential instructions to said central processing unit during a single memory cycle," TPL alleges:

> The ROM [i.e., read-only-memory] stores a mixture of routines of 32-bit ARM code with one instruction per 32-bit word and routines of Thumb code with two instructions per word. Each external fetch draws either one 32-bit ARM

> instruction or two 16-bit Thumb instructions. ARM instructions flow into the core pipeline in the usual way. However, in Thumb state, one Thumb instruction goes into the pipeline while the other is stored on a 16-bit latch, which is effectively a one-instruction prefetch buffer. At the next fetch, this stored instruction is immediately available to the core.

Chen Decl., Ex. 3, pp. 6 and 14 of 24 (emphasis added) (quoting ARM td., *An Introduction to Thumb*). TPL's Infringement Contentions rely on the above-quoted factual allegation to explain how the handling of Thumb instructions allegedly meets this claim element. This is the only allegation in TPL's Infringement Contentions that attempts to identify, with any degree of particularity, the mechanism by which the accused '749 products supply multiple instructions to the CPU. That mechanism, however, provides Thumb instructions from a prefetch buffer to the CPU one at a time.

As such, TPL is improperly attempting to accuse the exact system it disclaimed in order to obtain allowance of its claims. As noted above, TPL told the PTO that "[f]etching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation – the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'" Amendment, 01/19/2010, p. 26 of 58, Chen Decl., Ex. 1 (emphasis added). As the Federal Circuit has noted, "[t]he public has a right to rely on the assertions made by a patent applicant to secure allowance of its claims. Post-hoc, litigation-inspired argument cannot be used to reclaim subject matter that the public record in the PTO clearly shows has been abandoned." *Desper Prods., Inc.*, 157 F.3d at 1340. In this case, the only allegation made by TPL is to the exact system that it abandoned. Infringement, either literally or under the doctrine of equivalents, therefore cannot be established as a matter of law. Summary judgment with respect to the accused '749 products should therefore be granted.

B. The Accused '336 and '148 Products Do Not Infringe the '336 and '148 Patents, Respectively.

HTC and the other declaratory judgment plaintiffs have proposed constructions for a number of related claim terms pertaining to the component recited in the claims of the '336 and '148 patents, which the have generally been referred to as the "ring oscillator" related terms. The

construction of these terms is fully briefed in HTC's responsive and sur-reply claim construction briefs. Doc. No. 243 at 2-8; Doc. No. 265-1. Those terms, and the claims of the '336 and '148 patents, in which they appear, are shown in the following chart:

Patent	Claim Term	Claims
'336	An entire ring oscillator variable speed system clock in said single integrated circuit	1, 11
	An entire oscillator disposed upon said integrated circuit substrate	6, 13
	Providing an entire variable speed clock disposed upon said integrated circuit substrate	10, 16
'148	A *ring oscillator* having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate[4]	4
	a *ring oscillator* having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said first substrate	11

Chen Decl., Ex. 4, pp. 6, 13, 23, 29, 36 and 46 of 50; Ex. 5, pp. 6-7 and 13-14 of 18.

A common characteristic of each of HTC's proposed constructions is that the claimed oscillator, ring oscillator and variable speed clock must be, among other things, non-controllable. Doc. No. 243 at 2:6-8 (construction of "ring oscillator"), 5:11-16 ("an entire ring oscillator variable speed system clock . . ."), 5:21-25 ("an entire oscillator . . ."), 6:1-6 ("an entire variable speed clock . . ."). This requirement of non-controllability derives from the clear and unequivocal disclaimers made during the reexamination of the '148 patent, in which TPL distinguished the voltage controlled oscillator ("VCO") of U.S. Patent No. 4,689,581 to Talbot based on the fact that the claimed ring oscillator was "non-controllable." Doc. No. 243 at 2-3 (quoting February 12, 2008 Interview Summary and February 26, 2008 Amendment).

Despite its representations to the PTO, however, TPL's Infringement Contentions against the accused '336 products and the accused '148 products only identify a phase-locked loop

[4] HTC has asked the Court to construe the term "ring oscillator" from the '148 patent. To provide fuller context, the phrases shown in the chart in the text for the '148 patent reflect the entire phrase in which "ring oscillator" (shown in italics with underlining) appears.

("PLL") – that TPL admits indicates a *controllable* oscillator – as the structure that allegedly meets the "ring oscillator" related elements listed above. TPL's Infringement Contentions then, in order to explain how the PLL allegedly meets the ring oscillator elements, makes the following statement: "The presence of a PLL indicates the presence of a ring oscillator, either a voltage controlled oscillator ('VCO') or current controlled oscillator ('ICO')." Chen Decl., Ex. 4, p. 6 of 50; Ex. 5, p. 7 of 18 (emphasis added).

As TPL's contentions suggest, a voltage *controlled* oscillator or a current *controlled* oscillator is an oscillator that is "controlled." TPL's own expert also acknowledged as much when he admitted that a voltage controlled oscillator (such as the one in Talbot) "could be **controlled** by voltage or current." *See* Oklobdzija Depo. 12/22/2010 at 354:14-19, Chen. Decl., Ex. 6 (emphasis added). An oscillator that is controlled by voltage or current is certainly not "non-controllable." Summary judgment of non-infringement should therefore be granted with respect to the accused '336 products and the accused '148 products.

IV. CONCLUSION

For the foregoing reasons, HTC respectfully requests that the Court grant HTC's Motion in its entirety.

Dated: April 8, 2011

Respectfully submitted,

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